Optinet Technology Co., Ltd
Add: 4th Floor Xiufeng Industrial Park, Buji Street, Longgang District, Shenzhen,China 518112
Tel: +86-755-28471034 Fax:+86-755-61824579
www.optinetec.com sales@optinetec.com

OP-QSFP-DD-SR8

400G QSFP-DD SR8, 850nm, 100m on MMF, MPO16

FEATURES

- Hot-pluggable QSFP-DD form-factor
- Commercial temperature range of 0°C to 70°C
- Maximum link length of 100m on OM4 MMF with KP4 FEC
- Single 3.3V power supply
- Power dissipation < 10W
- MPO-16 APC connector

APPLICATION

- 400G 100m on MOE with FEC

Absolute Maximum Ratings

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	-0.3	-	3.6	V
Storage Temperature	TS	-40	-	+85	ºC
Maximum Supply Voltage	Vcc	-0.5	-	3.6	V
Operating Relative Humidity	RH	+5	-	+85	%
Receiver Damage Threshold per Lane	P_{RDMG}	+5			

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tcase	0	-	+70	ºC
Power Dissipation	Pd	-	-	10	w

Electrical Characteristics

Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling rate (each lane)	SR	GBPS	26.5625 ± 100 ppm			
Differential data input voltage per lane	Vin,pp,diff	mV	900	-	-	
Differential termination mismatchal	-	%	-	-	10	
Single-ended voltage tolerance range	-	V	-0.4	-	3.3	

DC common mode voltage	-	mV	-350	-	2850	
Receiver						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Differential output voltage	-	mV	-	-	900	
Near-end ESMW (Eye symmetry mask width)	-	UI	0.265	-	-	
Near-end Eye height, differential (min)	-	mV	70	-	-	
Far-end ESMW (Eye symmetry mask width)	-	UI	0.2	-	-	
Far-end Eye height, differential (min)	-	mV	30	-	-	
Differential termination mismatch	-	%		-	10	
Transition time (min, 20% to 80%)	-	ps	9.5	-	-	
DC common mode voltage	-	mV	-350	-	2850	

Optical Characteristics

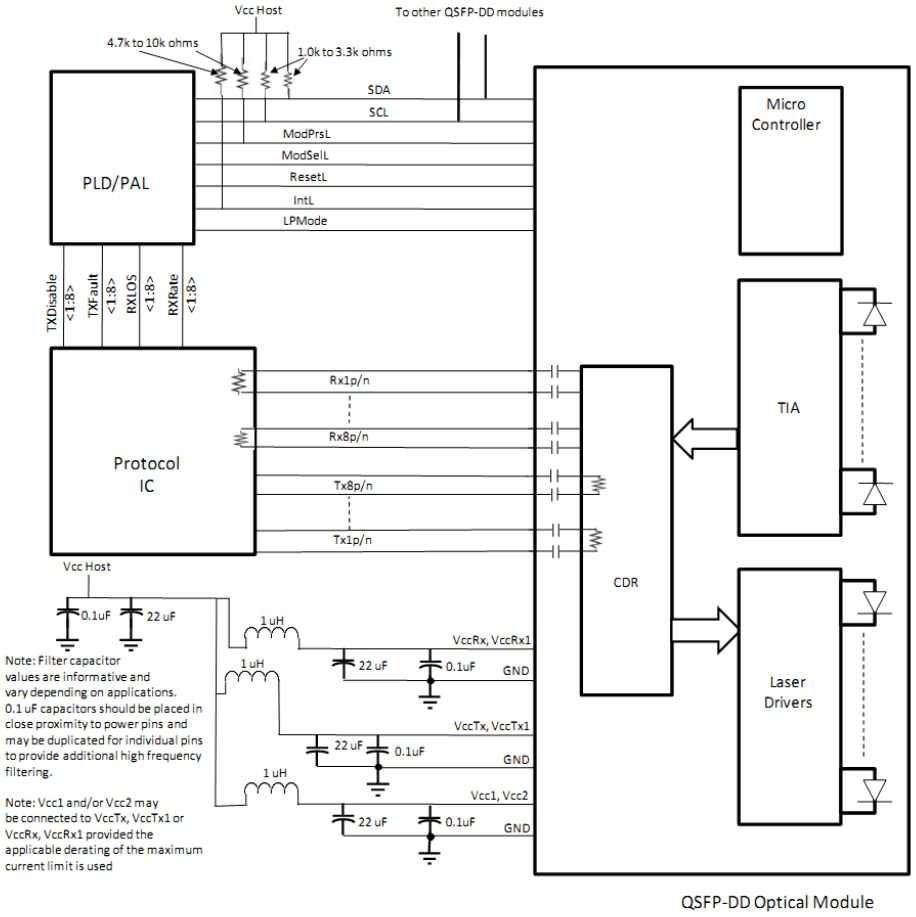
Parameter	Symbol	Unit	Min	Typ	Max	Notes
Transmitter						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Modulation format	-	-	PAM4			
Lane wavelength	λ	nm	840	850	860	
RMS spectral width	Δλ	nm	-	-	0.6	
Average launch power, each lane	-	dBm	-6.5	-	4	
Outer Optical Modulation Amplitude (OMAouter), each lane	-	dBm	-4.5	-	3	1
Launch power in OMA outer minus TDECQ, each lane	-	dBm	-5.9	-	-	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	-	dB	-	-	4.5	
Average launch power of OFF transmitter, each lane	-	dBm	-	-	-30	
Extinction ratio	-	dB	3	-	-	
Transmitter transition time, each lane	-	ps	-	-	34	
Optical return loss tolerance	-	dB	-	-	12	
Receiver						
Signaling rate (each lane)	SR	GBd	26.5625 ± 100 ppm			
Modulation format	-	-	PAM4			
Lane wavelength	λ	nm	840	850	860	
Damage threshold, each lane	P_{IN}	dBm	5	-	-	
Average receive power, each lane	-	dBm	-8.4	-	4	
Receive power (OMAouter), each lane	-	dBm	-	-	3	

Receiver sensitivity (OMAouter), each lane	-	dBm	-	-	Max(6.5,SEC Q-7.9)	2
LOS Assert	-	dBm	-30	-	-10	
LOS De-Assert	-	dBm	-	-	-9	
LOS Hysteresis	-	dB	0.5	-	-	

Note:

1. **Even if the TDECQ < 1.4 dB, the OMAouter (min) must exceed this value.**
2. **Bit Error Ratio < $2.4x10^{-4}$, Pattern PRBS31Q**

Recommended Interface



QSFP-DD Optical Module

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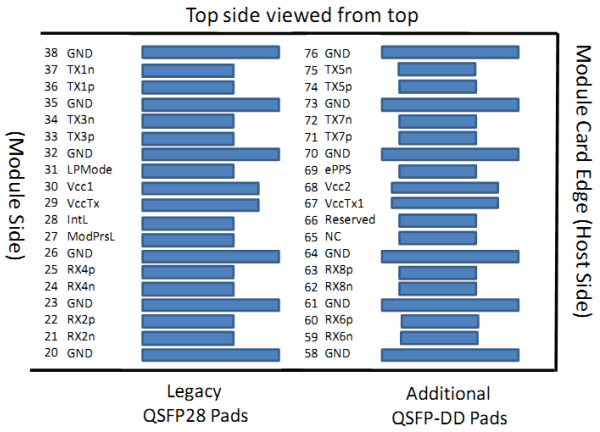
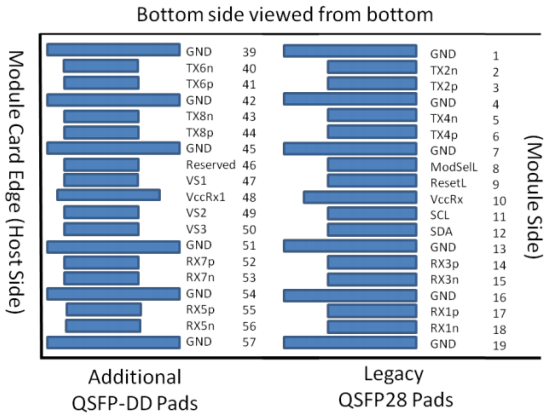
PIN Definition





Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

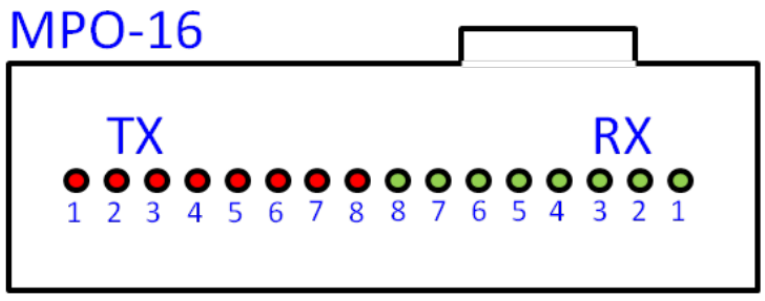
Note: 1. Circuit ground is internally isolated from chassis ground.

Memory Map

Compatible with QSFP-DD CMIS rev 4.0.

Optical Interface arrangement

The optical port is a male MPO connector receptacle, with fiber lane assignments as shown in below:



Optical interface arrangement Lens upwards

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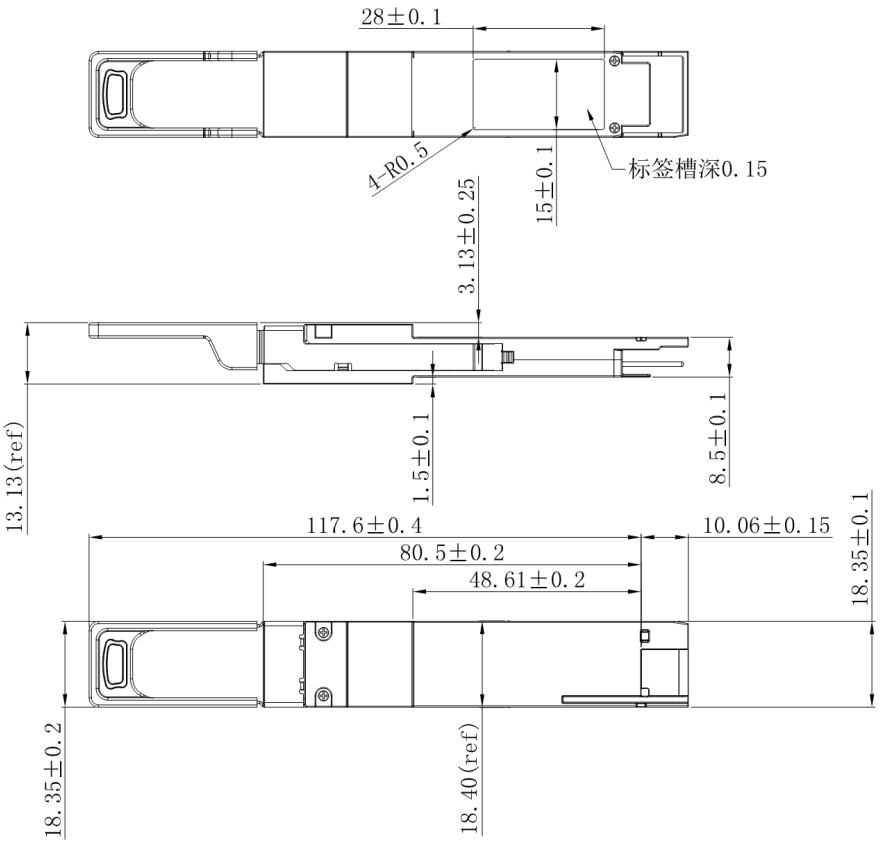
Mechanical Dimension

OP-QSFP-DD-SR8 QSFP-DD transceivers are compatible with the QSFP-DD Type 2 Specification for pluggable form factor modules.

Unit mm



Ordering information

Part Number	Product Description
OP-QSFP-DD-SR8	400G QSFP-DD SR8, 100m 850nm MPO16 DOM